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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,488	03/29/2004	Jun Yoshida	107337-00058	8887
4372	7590	02/28/2006	EXAMINER	
ARENT FOX PLLC 1050 CONNECTICUT AVENUE, N.W. SUITE 400 WASHINGTON, DC 20036				NGUYEN, DILINH P
		ART UNIT		PAPER NUMBER
		2814		

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,488	YOSHIDA ET AL.	
	Examiner DiLinh Nguyen	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 09 December 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-8 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Mori (U.S. Pat. 5949098).

Mori discloses a semiconductor device having a multilayer wiring structure, comprising:

a first power line 350 connected to a bypass capacitor C32 or C33;

a second power line 330 from which a part corresponding to a position of said bypass capacitor C33 is removed; and

a contact (341 or 342) for connecting said first power line and said second power line (fig. 3, column 4, lines 40 et seq.).

- Regarding claim 2, Mori discloses that a plurality of said contacts (341 and 342) is provided (fig. 3).
- Regarding claim 3, Mori discloses that the contact is attached to an end of the second power line 330 (fig. 3).
- Regarding claim 8, Mori discloses that the second power line 330 is installed in an upper wiring layer than the first power line 350 (fig. 3).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (U.S. Pat. 5949098) in view of Applicant Admitted Prior Art [AAPA] (figs. 3-4).

• Regarding claims 5-6, Mori substantially discloses all the limitations as claimed above except for the bypass capacitor is installed close to a circuit which is supplied with power, wherein the circuit is an I/O cell installed around a semiconductor tip.

However, AAPA (figs. 3-4) discloses a semiconductor device having a multilayer wiring structure, comprising:

a bypass capacitor 101 is installed close to a circuit 114 which is supplied with power and wherein the circuit 114 is an I/O cell 114a and 114b installed around a semiconductor tip 112 (fig. 4). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Takizawa by having an I/O cell installed around a semiconductor tip, as taught by AAPA (figs. 3-4), in order to effectively eliminate noise on the power lines for the semiconductor package (page 4, lines 17-19).

• Regarding claim 4, it would have been obvious to one having ordinary skill in the

art to have the contact is made wider than the power line to improve the electrical contact for the wiring structure.

- Regarding claim 7, AAPA discloses that the bypass capacitor is a transistor comprising: a gate electrode 101d formed on a semiconductor substrate 101a through a gate insulating film; and source/drain regions 101b and 101c formed on the semiconductor substrate with said gate electrode inserted therebetween; and said first power line 105 is connected to one of said source/drain regions and said gate electrode of said transistor (fig. 3).
- Regarding claim 8, AAPA discloses the second power line 103 is installed in an upper wiring layer than said first power line 105 (fig. 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DLN



HOAI PHAM
PRIMARY EXAMINER